Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1. (currently amended) A method of testing a semiconductor wafer, the semiconductor wafer having a plurality of die that contain static random access memory (SRAM) arrays, comprising the steps of:

   (a) coupling an array of probes to the semiconductor wafer; ~~and thereafter~~

   (b) applying a voltage difference across ~~a plurality of adjacent bitline pairs and/or worldine pairs~~ a pair of closely spaced wordlines or bitlines of one or more static random access memory (SRAM) arrays ~~of at least one die of the semiconductor wafer~~, wherein the voltage difference across the pair of closely spaced wordlines or bitlines exceeds a voltage difference that the wordlines or bitlines would experience in normal operation; ~~the voltage being larger than an operational supply voltage for~~ of ~~the one or more SRAM arrays, to thereby induce failure of metal stringers or defect;~~ and

   (c) identifying whether electrical shorting occurs across said pair of closely spaced wordlines or bitlines.

2. (currently amended) The method of claim 1, further comprising the step of simultaneously applying the voltage difference across respective pairs of substantially all parallel bitline pairs and/or wordline pairs of the one or more SRAM arrays.

3. (currently amended) The method of claim 1, further comprising the step of simultaneously applying a voltage across respective pairs of substantially all parallel bitline pairs and/or wordlines pairs of the one or more SRAM arrays of more than one die of the semiconductor wafer.

4. (currently amended) The method of claim 1, further comprising the step of applying the voltage difference across other adjacent, parallel metal lines of the one or more SRAM arrays.

5. (currently amended) The method of claim 1, further comprising the step of applying the voltage difference at a magnitude of equal to or greater than two times the operational supply voltage.

6. (currently amended) The method of claim 2, further comprising the step of applying the voltage difference at a magnitude of equal to or greater than two times the operational supply voltage.

7. (currently amended) The method of claim 3, further comprising the step of applying the voltage difference at a magnitude of equal to or greater than two times the operational supply voltage.

8. (currently amended) The method of claim 4, further comprising the step of applying the voltage difference at a magnitude of equal to or greater than two times the operational supply voltage.

9. (currently amended) The method of claim 1, further comprising the step of prerforming step b at an elevated temperature.

10. (currently amended) The method of claim 9, further comprising the step of applying the voltage difference at a magnitude of equal to or greater than two times the operational supply voltage.

11. (currently amended) The method of claim 3, further comprising the step of prerforming step b at an elevated temperature.

12. (currently amended) The method of claim 4, further comprising the step of prerforming step b at an elevated temperature.

13. (currently amended) A semiconductor wafer having one or more die with a static random access memory (SRAM) array integrated therein, comprising:

a test circuit integrated with the SRAM array; and

connections that couple said test circuit to the SRAM array;

wherein during probing, said test circuit applies a voltage difference across a plurality of adjacent bitline pairs and/or worldine pairs of the SRAM

array, the voltage difference being larger than an operational supply voltage for the SRAM array, to identify whether electrical shorting occurs across one or more of said plurality of adjacent bitline pairs and/or wordline pairs., ~~to thereby induce failure of metal stringers or defects.~~